v. creating an analog subtraction signal from said time domain digital signal using a digital to analog converter,

vi. obtaining an error signal by subtracting said analog subtraction signal from said analog signal input into the subtractor,

vii. converting said error signal into a second time domain digital output signal using a second ADC (ADC2),

viii. transforming said second time domain digital output signal into a second frequency domain signal, and

ix. equalizing said second frequency domain signal to obtain a second equalized frequency domain signal and subtracting said second equalized frequency domain signal from said first frequency domain signal,

and wherein said step of recombining includes

x summing vectorially said first equalized time domain signal and said second equalized frequency domain signal to provide a frequency domain digital output signal, and

xi. transforming said frequency domain digital output signal into a time domain signal using an inverse transform to obtain said final output signal.

Respectfully Submitted,

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